CPIT210 : Computer Organization and Architecture

Course Lectures by Prof. Mohamed Khamis

Part 1: Logic Design

Tutorial

by

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Tutorial 1: Introduction & Implementation of Algebraic Functions:

A Brief Review of Number Systems:

1. Two's complement notation of Binary numbers:

The two's complement of a binary integer is formed by reversing its bits and adding 1.

Example: 000111110011 → 111000001101

2. Two's complement notation of Hexadecimal numbers:

To form the two's complement of a hexadecimal integer, reverse all bits and add 1. An easy way to reverse all bits of a hexadecimal digit is to subtract the digit from 15 (F). Here are several examples of a hexadecimal integers converted to their two's complements:

6A3D →(F-6)(F-A)(F-3)(F-D) → 95C2 → 95C2 + 1 → 95C3
95C3 → (F-9)(F-5)(F-C)(F-3) →6A3C →6A3C + 1 → 6A3D
DE10 → (F-D)(F-E)(F-1)(F-0) →21EF →21EF + 1 → 21F0

3. Converting unsigned decimal to binary

To translate an unsigned decimal integer into binary, repeatedly divide the decimal value by 2, saving each remainder as a binary digit.
Example: 37 → 00100101

4. Converting unsigned binary to decimal

Example: 00001001 → $(1 \times 2^0) + (1 \times 2^3) = 9$

5. Converting signed decimal to binary

Here are the steps to follow:
1- Convert the absolute value of the decimal integer to binary.
2- If the original integer was negative, form the two's complement of the binary number.
Example: -43 → 11010101

1. The binary representation of the unsigned 43 is 00101011.
2. Because the original value was negative, we form the two's complement of 00101011 which is 11010101. This is the representation of -43 decimal.

6. Converting signed binary to decimal

Here are the steps to follow:

- If the highest bit is a 1, it is currently stored in a two's complement notation. You must form its two's complement notation a second time to get its positive equivalent. Then you can convert this new number to decimal as if it were an unsigned binary integer.
- If the highest bit is a 0, you can convert it to decimal as it were an unsigned binary integer.

For example, signed binary 11110000 has a 1 in highest bit, indicating that is a negative integer.
Step 1: form the twos complement → 00010000
Step 2: convert to decimal → 16
step 3: infer the decimal value → -16

7. Converting hexadecimal to binary

Each digit in a hexadecimal integer represents four binary bits:

Example: 0AB3 → 0000 1010 1011 0011

8. Converting binary to hexadecimal

Each four bits in a binary integer represents a single hexadecimal integer.

Example: 0000 0101 0011 1010 → 053A

9. Converting unsigned decimal to hexadecimal

To convert an unsigned decimal integer to hexadecimal, repeatedly divide the decimal value by 16, and keep each remainder as a hexadecimal digit.
For example: 422 → $(1A6)_{hex}$

Division	Quotient	Remainder
422 / 16	26	6
26 / 16	1	A (10)
1 / 16	0	1

10. Converting Signed decimal to hexadecimal

To convert a signed decimal integer to hexadecimal do the following:

- Convert the absolute value of the decimal integer to hexadecimal.
- If the decimal integer was negative, form the two's complement of the hexadecimal number.

Example: -43 → D5, here are the steps I did to convert it:

Step 1: convert 43 to hexadecimal → 2B
Step 2: because the decimal integer is negative, we will form the twos complement of a hexadecimal. 2B → D4 +1 → D5

11. Converting signed hexadecimal to decimal

To convert a signed hexadecimal integer to a decimal, do the following:

- If the hexadecimal integer is negative, form its two's complement; otherwise, retain as is.
- Using the integer from the previous step, convert it to decimal. If the original value was negative, attach a minus sign to the begging of the decimal integer.

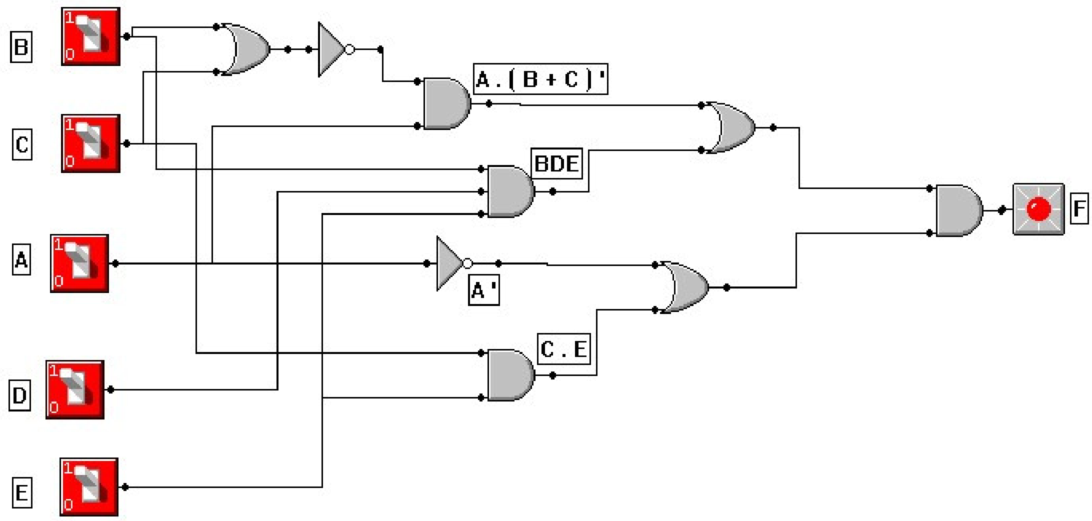
Important Note:
You can tell if a hexadecimal integer is positive or negative by inspecting its most significant (highest) digit. If the digit is >=8, the number is negative; if the digit is <=7, the number is positive. For example, hexadecimal 8A21 is negative, and 7FD9 is positive.

For example, signed hexadecimal A02F has an A in highest digit, indicating that is a negative integer.
Step 1: form the twos complement of a hexadecimal → 5FD0 + 1 → 5FD1
Step 2: convert to decimal → $(1 \text{ X } 16^0) + (13 \text{ X } 16^1) + (15 \text{ X } 16^2) + (5 \text{ X } 16^3)$= 24529
step 3: infer the decimal value → -24529

Q1] Show a block diagram of a system using AND, OR, and NOT gates to implement the following function:

F=(A (B + C)’ + B D E) (A’ + C E)

Answer:



Q2] Simply the following expression in:

(i) Sum of Product. (ii) Product of Sum.

a) X’ Z’ + Y’ Z’ + Y Z’ + X Y
b) A C’ + B’ D’ + A’ C D + A B C D
c) (A’ + B’ + D’) (A + B’ + C’) (A’ + B + D’) (B + C’ + D’)

Answer:

a) X’ Z’ + Y’ Z’ + Y Z’ + X Y

X	Y	Z	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

S.O.P F= X’ Y’ Z’ + X’ Y Z’ + X Y’ Z’ + X Y Z’ + X Y Z

P.O.S F= (X’ Y’ Z)’ . (X’ Y Z)’ .(X Y’ Z)’ = (X + Y + Z’) (X+ Y’ + Z’) (X’ + Y + Z’)

b) A C’ + B’ D’ + A’ C D + A B C D

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

S.O.P F=A’ B’ C’ D’ + A’ B’ C D’+ A’ B’ C D + A’ B C D + A B’ C’ D’ + A B’ C’ D
+ A B’ C D’ + A B C’ D’ + A B C’ D + ABCD

P.O.S F= (A’ B’ C’ D)’ . (A’ B C’ D’)’ .(A’ B C’ D)’ (A’ B C D’)’ (A B’ C D)’ (A B C D’)’
=(A+B+C+D’) (A+B’+C+D) (A+B’+C+D’) (A+B’+C’+D) (A’+B+C’+D’) (A’+B’+C’+D)

c) (A’ + B’ + D’) (A + B’ + C’) (A’ + B + D’) (B + C’ + D’)

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

S.O.P F=A’ B’ C’ D’ + A’ B’ C’ D+ A’ B’ C D’ + A’ B C’ D’ + A’ B C’ D + A B’ C’ D’ + A B’ C D’ + A B C’ D’ + A B C D’

P.O.S F= (A’ B’ C D)’ . (A’ B C D’)’ .(A’ B C D)’ (A B’ C’ D)’ (A B’ C D)’ (A B C’ D)’ (A B C D)’
=(A+B+C’+D’) (A+B’+C’+D) (A+B’+C’+D’) (A’+B+C+D’)
(A’+B+C’+D’) (A’+B’+C+D’) (A’+B’+C’+D’)

Q3]

I) Design the following functions using only NAND gates :
   a) X Y’ + Y Z + X’ Y’ Z’
   b) X’ Y + (X + Z’) (Y + Z)

II) Redesign the functions above using only NOR gates.

Answer

I) Using only NAND gates.

a) (X Y’ + Y Z + X’ Y’ Z’)’ ‘

= ((X Y’)’ . (Y Z)’ . (X’ Y’ Z’)’)’

b) X’ Y + (X + Z’) (Y + Z)

= (X’ Y + (X + Z’) (Y + Z))’ ‘

= ((X’ Y)’ . ((X + Z’) (Y + Z))’)’

= ((X’ Y)’ . ((X + Z’)’ ‘ (Y + Z)’ ‘)’)’

= ((X’ Y)’ . ((X’ . Z)’ (Y’ . Z) ‘)’)’

II) Using only NOR gates.

a) X Y’ + Y Z + X’ Y’ Z’
= (X Y’)’ ‘ + (Y Z)’ ‘ + (X’ Y’ Z’)’ ‘
= ((X’ +Y)’ + (Y’ + Z’)’ + (X+ Y+ Z)’)’ ‘

b) X’ Y + (X + Z’) (Y + Z)

= (X’ Y)’ ‘ + ((X + Z’) (Y + Z))’ ’

= (X+ Y’)’ + ((X + Z’)’+ (Y + Z)’)’

= ((X+ Y’)’ + ((X + Z’)’+ (Y + Z)’)’) ‘ ‘

Tutorial 2: The Karnaugh Map & an Introduction to Combinational Circuits

Q1] Design a combinational circuit that converts a binary number of four bits to a decimal number in BCD. Note that the BCD number is the same as the binary number as long as the input is less than or equal to 9. The binary number from 1010 to 1111 converts into BCD number from 1 0000 to 1 0101.

Answer:

a3	a2	a1	a0	z3	z2	z1	z0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1
1	1	0	0	0	0	1	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	0	0
1	1	1	1	0	1	0	1

a0 a1 \ a2 a3	00	01	11	10
00				
01				
11	1	1	1	1
10	1	1	1	1

Z0= a0

a0 a1 \ a2 a3	00	01	11	10
00			1	
01	1			1
11	1			1
10			1	

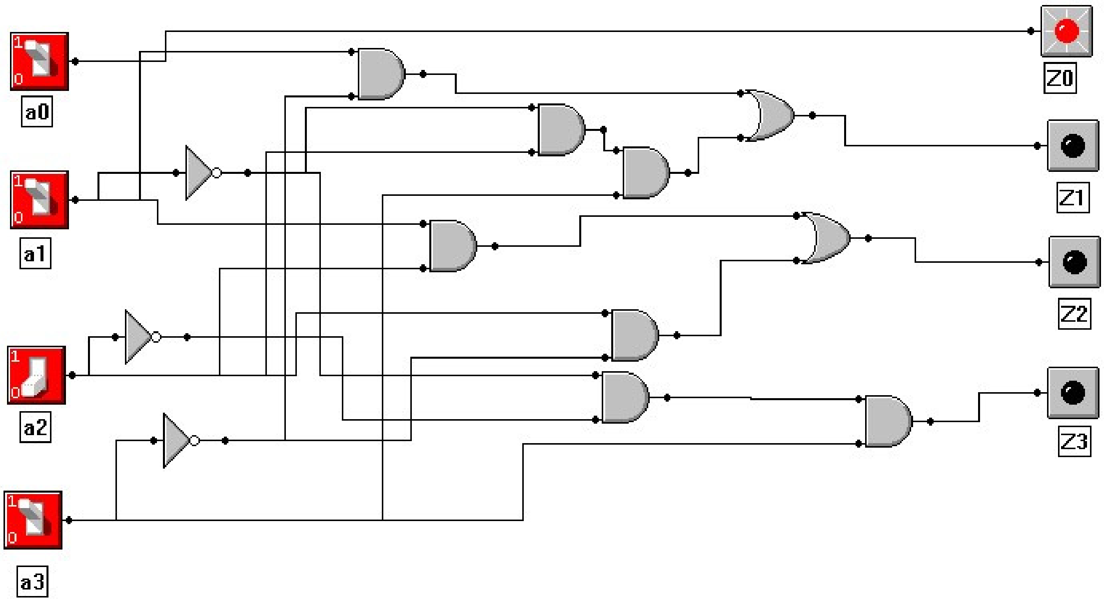
Z1= a1 a3’ + a1’ a2 a3

a0 a1 \ a2 a3	00	01	11	10
00				1
01			1	1
11			1	1
10				1

Z2= a1 a2 + a2 a3’

a0 a1 \ a2 a3	00	01	11	10
00		1		
01				
11				
10		1		

Z3= a1’ a2’ a3



0-1Decimal To BCD Circuit

Q2] Use a karnaugh map to minimize the following expression in :

(i) Product of Sum expression. (ii) Sum of product expression

a) (A + B + C) (A + B + C’) (A + B’ + C) (A + B’ + C’) (A’ + B’ + C)
b) (B + C + D) (A + B + C’ + D) (A’ + B + C + D’) (A + B’ + C + D) (A’ + B’ + C + D)
c) (A’ + B’ +C +D)(A + B’ + C + D)(A + B + C + D’)(A + B + C’ + D’)(A’ + B +C + D’)(A + B + C' +D)

Answer:

a) (A + B + C) (A + B + C’) (A + B’ + C) (A + B’ + C’) (A’ + B’ + C)

AB \ C	0	1
00	0	0
01	0	0
11	0	1
10	1	1

P.O.S = A (B’ + C)

S.O.P= A C + A B’

b) (B + C + D) (A + B + C’ + D) (A’ + B + C + D’) (A + B’ + C + D) (A’ + B’ + C + D)

A B \ C D	00	01	11	10
00	0	1	1	0
01	0	1	1	1
11	0	1	1	1
10	0	0	1	1

P.O.S = (C + D) (A + B + D) (A’ + B + C)

S.O.P= A’ D + B D + B C + A C

C) (A' + B' +C +D)(A + B' + C + D)(A + B + C + D')(A + B + C' + D')(A' + B +C + D')(A + B + C' +D)

AB \ CD	00	01	11	10
00	1	0	0	0
01	0	1	1	1
11	0	1	1	1
10	1	0	1	1

P.O.S = (B' + C + D) (B + C + D') (A + B + C')

S.O.P= B' C' D' + B D + B C + A C

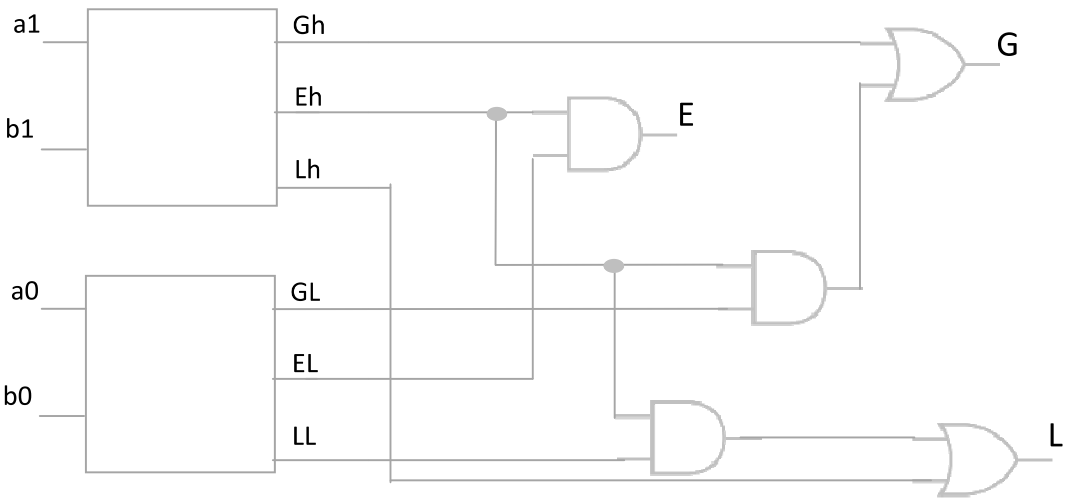
Q3] Design 2-bit Comparator using the block diagram of the 1-bit comparator.

Answer:

G= Gh + Eh Gl

E= Eh El

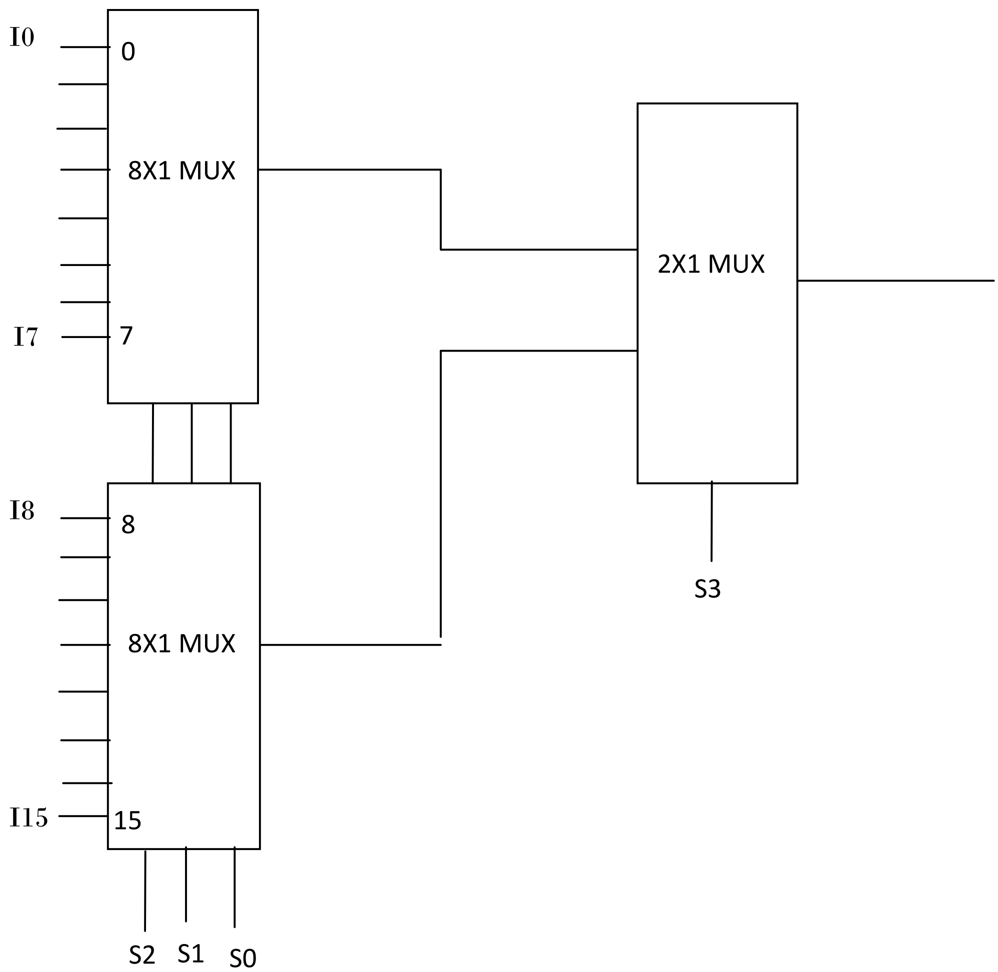
L= Lh + Eh Ll



Tutorial 3: Large Combinational Circuits: Multiplexers

Q1] Construct 16X1 multiplexer using two (8X1) and one (2X1) multiplexers. (use block diagram for each multiplexer).

Answer:

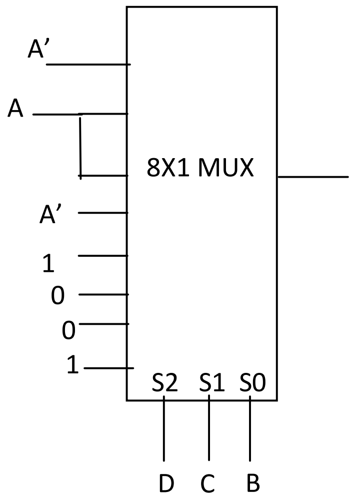


Q2] Implement the following Boolean function with an 8X1 multiplexer

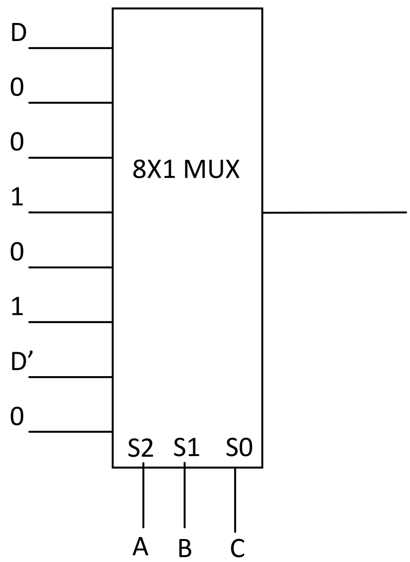
F(A,B,C,D)=0,3,5,6,8,9,14,15

Answer:

D	C	B	A	F	
0 0	0 0	0 0	0 1	1 0	A’
0 0	0 0	1 1	0 1	0 1	A
0 0	1 1	0 0	0 1	0 1	A
0 0	1 1	1 1	0 1	1 0	A’
1 1	0 0	0 0	0 1	1 1	1
1 1	0 0	1 1	0 1	0 0	0
1 1	1 1	0 0	0 1	0 0	0
1 1	1 1	1 1	0 1	1 1	1



Q3] An 8X1 MUX has inputs A,B and C connected to selection inputs S2, S1 and S0 respectively has inputs as in figure determine the Boolean function of the circuit.



Answer:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Note that D is LSB

F(D,C,B,A)= $\sum$ 1,6,7,10,11,12

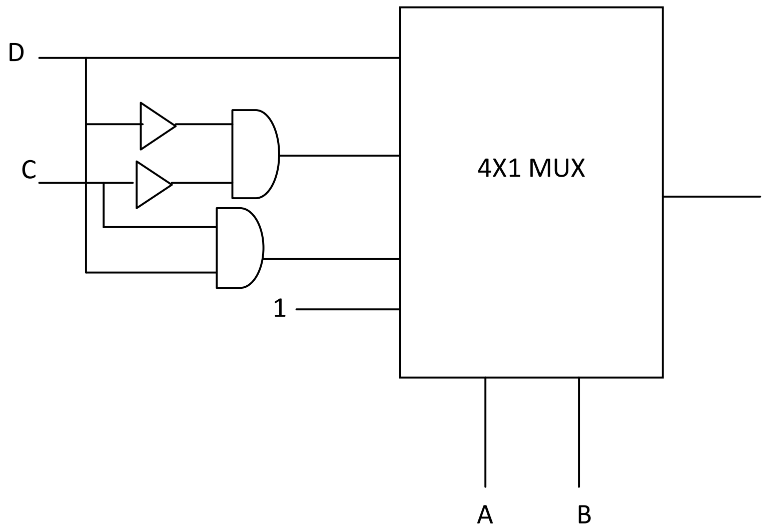
Q4] Implement the following Boolean function with 4X1 multiplexers and external gates. Connect inputs A and B to the selection lines, the input requirements for the four data lines will be a function of variables C and D. These values are obtained by expressing F as a function of the four cases when AB=00, 01,10 and 11.

These function may have to be implemented with external gates.

F(A,B,C,D)=∑ 1,3,4,11,12,13,14,15

Answer:

A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	1	C’ + D + C D’
0	0	1	0	0	= D
0	0	1	1	1	
0	1	0	0	1	
0	1	0	1	0	C’ D’
0	1	1	0	0	
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	0	
1	0	1	0	0	C D
1	0	1	1	1	
1	1	0	0	1	
1	1	0	1	1	1
1	1	1	0	1	
1	1	1	1	1	



Another answer:

D	C	B	A	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

D	C	F
0	0	0
0	1	1
1	0	0
1	1	1

F0= C D’ + C D = C

D	C	F
0	0	1
0	1	0
1	0	0
1	1	1

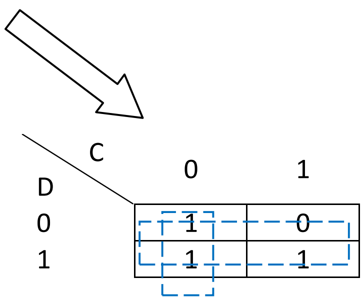
F1= C’ D’ + C D

D	C	F
0	0	0
0	1	0
1	0	0
1	1	1

F2= C D

D	C	F
0	0	1
0	1	0
1	0	1
1	1	1

F3= C’ + D

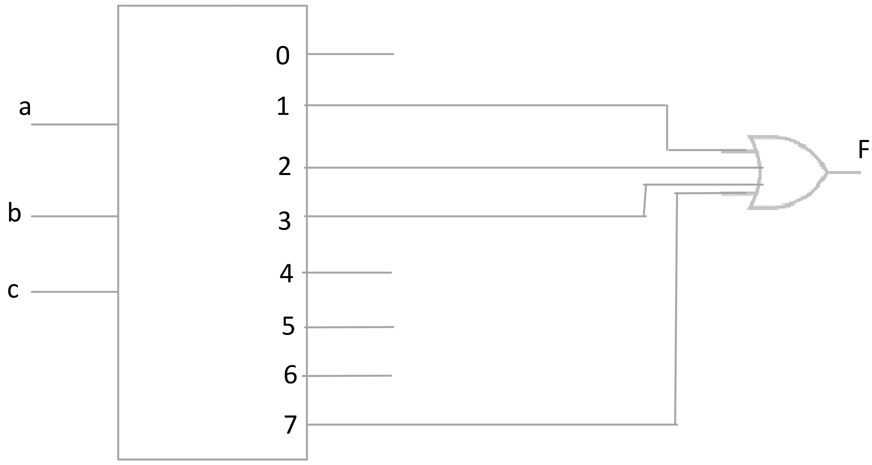


Tutorial 4: Large Combinational Circuits: Decoders & Encoders

Q1] Implement the following function using the Decoder:

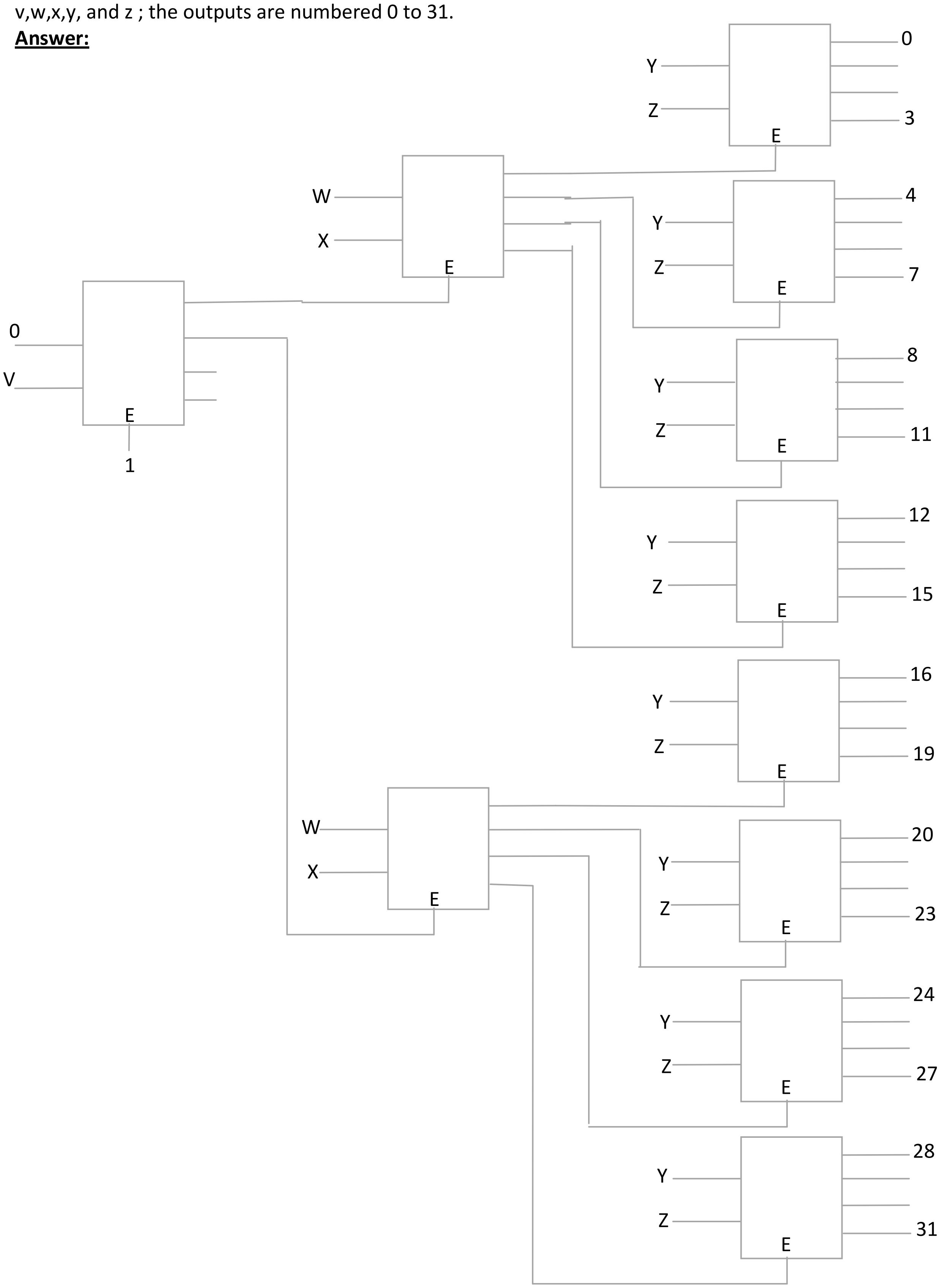
F(a,b,c) = ∑ 1, 2, 3, 7

Answer:



Q2] Design a 32-way active high decoder, using only the four-way decoders. The inputs are v,w,x,y, and z ; the outputs are numbered 0 to 31.

<u>Answer:</u>

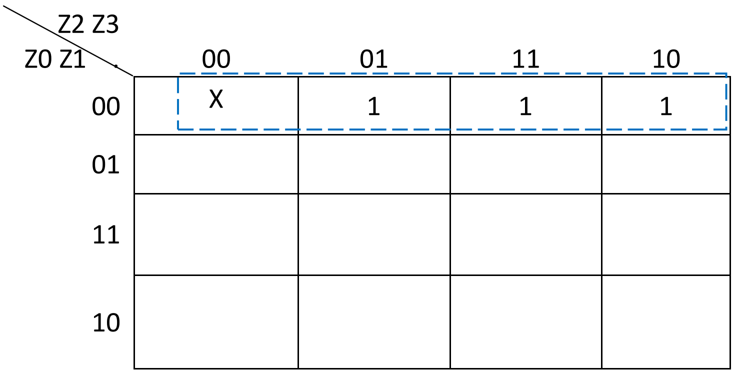


Q2] Design a priority encoder with four active high inputs Z0, Z1, Z2, and Z3 and three active high outputs, A and B indicating the number of the highest priority device requesting service, and N, indicating no active request. Input Z0 is the highest priority (and Z3 the lowest).

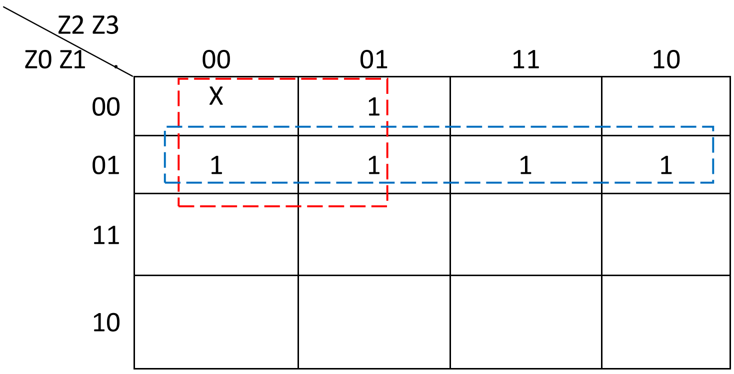
Answer:

Z0	Z1	Z2	Z3	A	B	N
0	0	0	0	X	X	1
1	X	X	X	0	0	0
0	1	X	X	0	1	0
0	0	1	X	1	0	0
0	0	0	1	1	1	0

N = Z0’ Z1’ Z2’ Z3’



A= Z0’ Z1’



B= Z0’ Z1 + Z0’ Z2’

Tutorial 5: The Design of Sequential Systems: Flip Flop Techniques

Q1] Design a Counter that counts up or down from 0 to 7, a control input U determines whether the counter is upward or downward, if U=1 the circuit counts upward with sequence 000,001,010,011,100,101,110,111 and the count repeats, if u=0 the circuit counts downward with sequence 111,110,101,100,011,010,001,000 and the count repeats.

Answer:

J	K	Q
0	0	No change
1	0	Set
0	1	Reset
1	1	Change

JK flip flop transition table

Q 0	Q+ 0	
0	0	no change
0	1	Reset

0 D

Q 0	Q+ 1	
1	0	set
1	1	change

1 D

Q 1	Q+ 0	
0	1	Reset
1	1	change

D 1

Q 1	Q+ 1	
0	0	no change
1	0	Set

D 0

Q	Q+	J	K
0	0	0	D
0	1	1	D
1	0	D	1
1	1	D	0

U	Q2	Q1	Q0	Q2+	Q1+	Q0+	J0	K0	J1	K1	J2	K2
1	0	0	0	0	0	1	1	D	0	D	0	D
1	0	0	1	0	1	0	D	1	1	D	0	D
1	0	1	0	0	1	1	1	D	D	0	0	D
1	0	1	1	1	0	0	D	1	D	1	1	D
1	1	0	0	1	0	1	1	D	0	D	D	0
1	1	0	1	1	1	0	D	1	1	D	D	0
1	1	1	0	1	1	1	1	D	D	0	D	0
1	1	1	1	0	0	0	D	1	D	1	D	1
0	0	0	0	1	1	1	1	D	1	D	1	D
0	0	0	1	0	0	0	D	1	0	D	0	D
0	0	1	0	0	0	1	1	D	D	1	0	D
0	0	1	1	0	1	0	D	1	D	0	0	D
0	1	0	0	0	1	1	1	D	1	D	D	1
0	1	0	1	1	0	0	D	1	0	D	D	0
0	1	1	0	1	0	1	1	D	D	1	D	0
0	1	1	1	1	1	0	D	1	D	0	D	0

U Q2 / Q1 Q0	00	01	11	10
00	1	1	1	1
01	d	d	d	d
11	d	d	d	d
10	1	1	1	1

J0= 1

U Q2 / Q1 Q0	00	01	11	10
00	1	1	1	1
01	d	d	d	d
11	d	d	d	d
10	1	1	1	1

K0= 1

Q1 Q0 \ U Q2	00	01	11	10
00	1	1	0	0
01	0	0	1	1
11	d	d	d	d
10	d	d	d	d

J1= U’ Q0’ + U Q0

Q1 Q0 \ U Q2	00	01	11	10
00	1	1	0	0
01	0	0	1	1
11	d	d	d	d
10	d	d	d	d

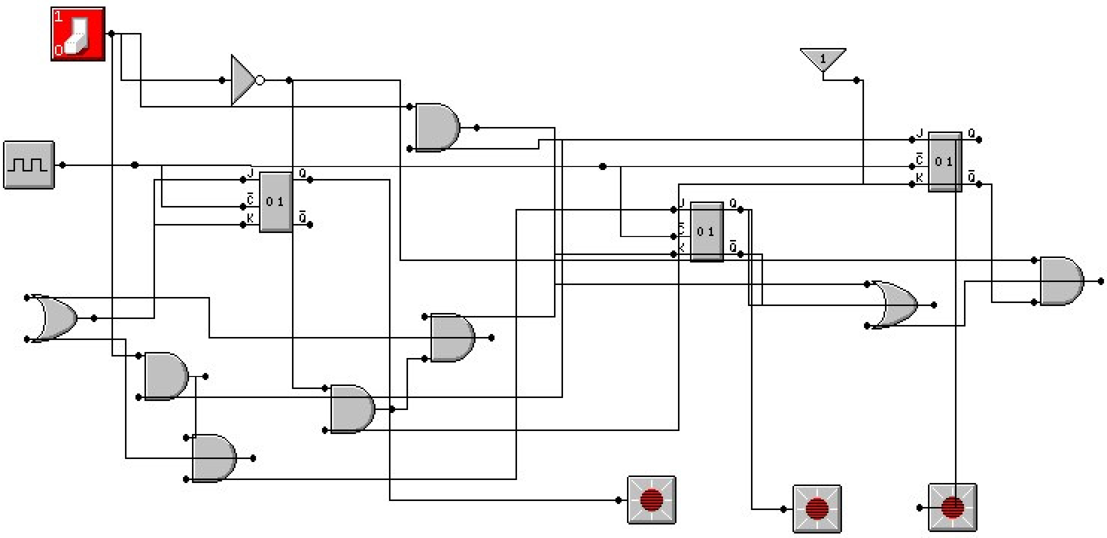
K1= U’ Q0’ + U Q0

Q1 Q0 \ U Q2	00	01	11	10
00	1	d	0	0
01	0	0	0	d
11	d	d	d	1
10	0	d	d	0

J2= U’ Q0’ Q1’ + U Q0 Q1

U Q2 / Q1 Q0	00	01	11	10
00	1	d	0	0
01	0	0	0	d
11	d	d	d	1
10	0	d	d	0

K2= U’ Q0’ Q1’ + U Q0 Q1



Q2] Design an odd counter that counts upward or downward as the following sequence of binary states 1,3,5,7 and for invalid states the counter will counts one (001).

Answer:

U	Q2	Q1	Q0	Q2+	Q1+	Q0+	J0	K0	J1	K1	J2	K2
1	0	0	0	0	0	1	1	D	0	D	0	D
1	0	0	1	0	1	1	D	0	1	D	0	D
1	0	1	0	0	0	1	1	D	D	1	0	D
1	0	1	1	1	0	1	D	0	D	1	1	D
1	1	0	0	0	0	1	1	D	0	D	D	1
1	1	0	1	1	1	1	D	0	1	D	D	0
1	1	1	0	0	0	1	1	D	D	1	D	1
1	1	1	1	0	0	1	D	0	D	1	D	1
0	0	0	0	0	0	1	1	D	0	D	0	D
0	0	0	1	1	1	1	D	0	1	D	1	D
0	0	1	0	0	0	1	1	D	D	1	0	D
0	0	1	1	0	0	1	D	0	D	1	0	D
0	1	0	0	0	0	1	1	D	0	D	D	1
0	1	0	1	0	1	1	D	0	1	D	D	1
0	1	1	0	0	0	1	1	D	D	1	D	1
0	1	1	1	1	0	1	D	0	D	1	D	0

U Q2 / Q1 Q0	00	01	11	10
00	1	1	1	1
01	d	d	d	d
11	d	d	d	d
10	1	1	1	1

J0= 1

Q1 Q0 \ U Q2	00	01	11	10
00	d	d	d	d
01	0	0	0	0
11	0	0	0	0
10	d	d	d	d

K0= 0

Q1 Q0 \ U Q2	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	d	d	d	d
10	d	d	d	d

J1= Q0

Q1 Q0 \ U Q2	00	01	11	10
00	d	d	d	d
01	d	d	d	d
11	1	1	1	1
10	1	1	1	1

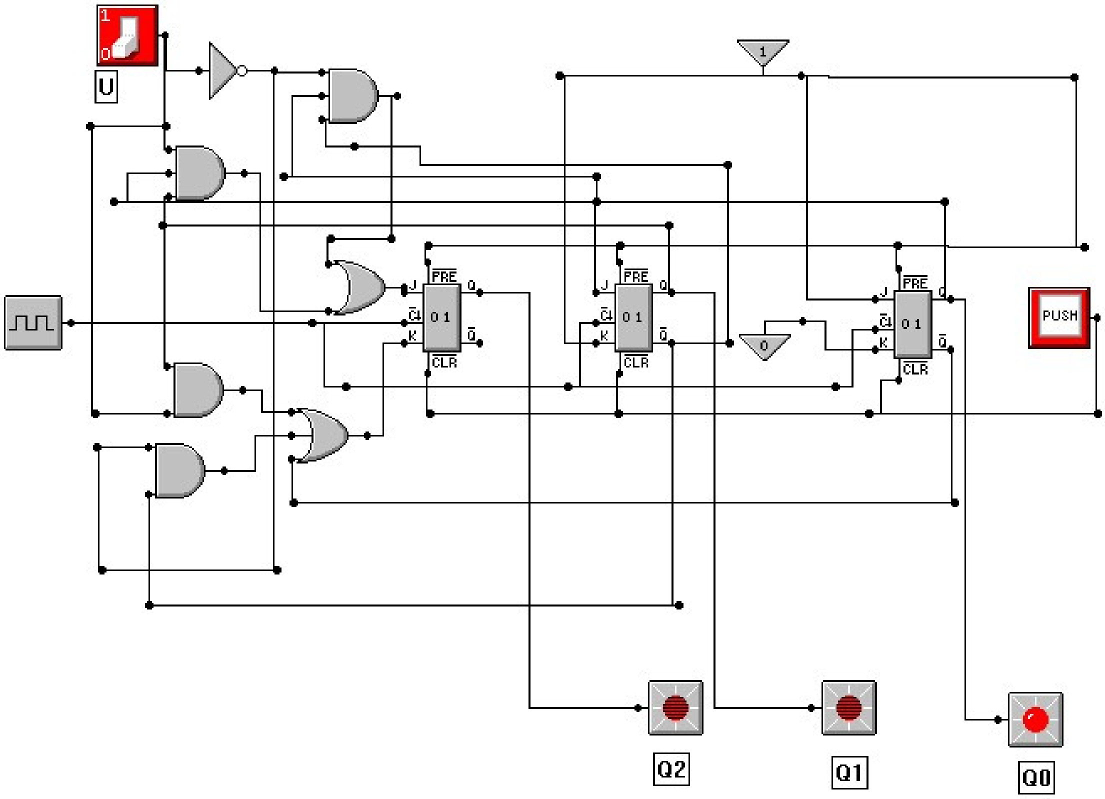
K1= 1

Q1 Q0 \ U Q2	00	01	11	10
00	0	d	d	0
01	1	d	d	0
11	0	d	d	1
10	0	d	d	0

J2= U’ Q0 Q1’ + U Q0 Q1

Q1 Q0 \ U Q2	00	01	11	10
00	d	1	1	d
01	d	1	0	d
11	d	0	1	d
10	d	1	1	d

K2=Q0’ + U’ Q1’ + U Q1


U
PUSH
Q2
Q1
Q0